Amendments to the Specification

Please replace the paragraph beginning on page 4, line 1 with the following amended paragraph:

There are three main alignment marks, as described above, and problems of the respective alignment marks and measures to solve the problems are the same for the three alignment marks. Thus, the mark for alignment and measurement will be described in the following. ~~Fig. 5 is a~~ Figs. 5A and 5B are schematic [[view]] views of a typical structure of the mark for alignment and measurement of a conventional semiconductor device. Fig. 5A shows a schematic plan view of the mark for alignment and measurement, and Fig. 5B shows a cross sectional view taken on a line 5B - 5B in ~~Fig. 51B - 1Bs shown in~~ Fig. 5A, the mark for alignment and measurement is formed of two patterns of an OUT-BOX 900 and an IN-BOX 910. The pattern shape of the OUT-BOX 900 is formed in a rectangular outside shape having a specified width and the pattern shape of the IN-BOX 910 is formed in a rectangular shape. The IN-BOX 910 is arranged inside the OUT-BOX 900.

Please replace the paragraph beginning on page 5, line 10 with the following amended paragraph:

~~Fig. 5~~ Fig. 5A is a drawing corresponding to a case where the first pattern layer is a layer in which a contact hole is formed and where the OUT-BOX is simultaneously formed at the time of etching the contact hole and where the IN-BOX is formed in the

following process. The structure shown in Fig. 5B is manufactured by the method to be described below. First, a contact hole is formed in an interlayer insulation film 901 in a contact hole etching process. Then, a barrier metal is formed of, for example, Ti/TiN (titan/ titan nitride) . Then, a tungsten film (hereinafter referred to as "W film") is formed by a tungsten chemical vapor deposition method (hereinafter referred to as "W-CVD method"). In the barrier metal and the W film, a metal film 902 is formed only inside the contact hole by the use of an etch back method or a chemical mechanical polishing method (hereinafter referred to as "CMP method"). At this time, in a case where the etch back method is used, as shown in Fig. 5B, a metal layer remains in the shape of a side wall in a mark region and in a case where the CMP method is used, the metal layer remains in the more expanded region. Thereafter, an interlayer insulation film 903 is formed and the IN-BOX is formed of the second pattern layer. A silicon nitride film, for example, is used for the interlayer insulation film 903. Alternatively, in some case, the first pattern layer is formed and then a capacitor electrode is directly formed without forming the interlayer insulation film 903. In this case, the insulation film 903 shown in Fig. 5B becomes a capacitor electrode film.

Please replace the paragraph beginning on page 6, line 12 with the following amended paragraph:

Even if the stepped portions formed in the shape of side wall are covered with the silicon nitride film or the capacitor electrode film, as shown in Fig. 5B ~~Fig. 5~~, W

(tungsten) is heavily oxidized to deform the shape of the alignment mark, as shown in Figs. 6A and 6B ~~Fig. 6~~, by the heat treatment performed in the oxygen atmosphere at the time of forming the ferrodielectric substance. Fig. 6A shows an example of deformed shape of the IN-BOX and Fig. 6B shows an example of deformed shape of the OUT-BOX. Both of them are photographs taken with an optical microscope. When the alignment mark is deformed in the shape, a function as the alignment mark is not performed, and further very serious problems in manufacturing the semiconductor device such as the occurrence and separation of particles in the following processes are caused. Moreover, Fig. 7 shows a photograph of cross section of an alignment mark portion oxidized by a focused ion beam (hereinafter referred to as "FIB") and shows a state where the W film is oxidized and expanded to break the upper layer film.

Please replace the paragraph beginning on page 7, line 11 with the following amended paragraph:

In addition to the above-mentioned problems of oxidation and separation of the alignment mark portion, in the pattern shape of the OUT-BOX 900 shown in ~~Fig. 5~~ Figs. 5A and 5B whose outside shape is rectangular, there is presented a problem that since the pattern widths of the corner portions become larger than the pattern widths of the sides portions, voids are apt to occur at the corner portions. The occurrence of voids results in increasing the amount of etch back or CMP when the W etch back or the W-CMP is performed in the later process and hence causes a reduction in uniformity in the

plane of a wafer.

Please replace the paragraph beginning on page 10, line 24 with the following amended paragraph:

Figs. 1A – 1C are illustrations ~~Fig. 1 is an illustration~~ showing the construction of an alignment mark of a semiconductor device in accordance with the first embodiment of the present invention. Fig. 1A is a schematic plan view, Fig. 1B is a cross sectional view taken along a line 1B -1B in Fig. 1A, and Fig. 1C is a cross sectional view taken along a line 1C - 1C in Fig. 1A.

Please replace the paragraph beginning on page 11, line 14 with the following amended paragraph:

Figs. 5A and 5B are illustrations ~~Fig. 5 is an illustration~~ showing the construction of an alignment mark of a conventional semiconductor device. Fig. 5A is a schematic plan view, and Fig. 5B is a cross sectional view taken along a line 5B - 5B in Fig. 5A.

Please replace the paragraph beginning on page 11, line 18 with the following amended paragraph:

Figs. 6A and 6B are photographs ~~Fig. 6 is a photograph~~, taken with an optical microscope, of such an alignment mark of a conventional semiconductor device that is deformed into a faulty shape by oxidation. Fig. 6A is an example relating to an IN-BOX

and Fig. 6B is an example relating to an OUT-BOX.

Please replace the paragraph beginning on page 12, line 18 with the following amended paragraph:

A semiconductor device in accordance with the first embodiment of the invention ~~embodiment~~ will be described with reference to Figs. 1A – 1C ~~Fig. 1~~. This semiconductor device is formed on a substrate and includes an alignment mark. ~~Fig. 1 shows~~ Figs. 1A – 1C show the construction of the alignment mark. Fig. 1A is a schematic plan view and Fig. 1B is a cross sectional view taken along a line 1B - 1B in Fig. 1A and Fig. 1C is a cross sectional view taken along a line 1C - 1C in Fig. 1A. The semiconductor device in the present embodiment includes alignment marks of an OUT-LINE 100 and an IN-LINE 110. The pattern shape of each of alignment marks of the OUT-LINE 100 and the IN-LINE 110 in a plane parallel to the plane of the substrate is formed in a shape including four sides obtained by eliminating four corners from a rectangle. However, the rectangle on which the pattern shape of the IN-LINE 110 is based on is smaller the rectangle on which the pattern shape of the OUT-LINE 100 is based and the IN-LINE 110 is located inside the OUT-LINE 100. All of the patterns constructing the OUT-LINE 100 and the IN-LINE 110 have a uniform width ranging from 0.6 μm to 0.8 μm and are formed of metal films, respectively, as will be described later.

Please replace the paragraph beginning on page 14, line 2 with the following amended paragraph:

The alignment marks shown in ~~Fig. 1~~ Figs. 1A – 1C are marks for alignment and measurement and are used in a case where a first pattern layer of an underlying layer is aligned with a second pattern layer to be formed hereafter. For example, the first pattern layer forms the OUT-LINE 100 and then the second pattern layer forms the IN-LINE 110. By measuring the marks for alignment, constructed of the OUT-LINE 100 and the IN-LINE 110, by means of an alignment measurement instrument, the amount of deviation from alignment of the first pattern layer relative to the second pattern layer is detected. In a case where the amount of deviation from alignment is larger than a specified value, the second pattern layer is totally removed and then another second pattern is formed by the use of an obtained alignment correction value.